

PATENT APPLICATION

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

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HIGH SPEED LOW POWER DATA TRANSFER SCHEME

5 This application claims priority from U.S. Provisional Patent Application No. 60/120,531, filed February 17, 1999, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

10 1. Field Of The Invention

 The present invention relates to a data transfer scheme, and more particularly, to a high speed and low power CMOS data transfer scheme.

15 2. Description Of The Prior Art

 Today's requirements for electronic circuits require high speed. Additionally, the circuits should be as small and simple as possible due to the ever increasing number of circuits that are crowding today's chip devices. Furthermore, circuits for data transfer should not be sensitive to circuit parameter mismatches, noise, and deviations in various applied voltages.

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SUMMARY OF THE INVENTION

 The present invention provides a high speed and low power CMOS data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier
25 that serves as a bus receiver.

 In accordance with one embodiment of the present invention, a data transfer arrangement includes two bus drivers, a voltage precharge source, a differential bus coupled to the bus drivers and to the voltage precharge source, and a latching sense amplifier coupled to the differential bus.

30 In accordance with another embodiment of the present invention, the latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

Thus, the present invention provides a data transfer arrangement that operates at a high speed and uses low power. The data transfer arrangement is faster because the bus voltage swing passes directly to high gain nodes of the cross-coupled latched amplifier. Additionally, the data transfer arrangement uses a lower number of stacked transistors coupled between the supply voltage and the high gain nodes when compared to the prior art. Additionally, the arrangement according to the present invention is less sensitive to deviations in voltage sources and the deviation of threshold voltage concerns of the input transistors. Additionally, the arrangement is less sensitive to circuit parameter mismatches, data bus common mode noise and power bus noises.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred embodiments below, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in the data transfer arrangement illustrated in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential V_{pr} (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vice versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level V_{pr} toward a more positive $V_{dd} - V_t$ (where V_t is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level V_{pr} towards a more negative level V_{ss} (ground). This provides a differential voltage: $+dV$ and $-dV$ from the precharging level V_{pr} between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference $2 * dV_{min}$ (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to V_{dd} and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned off and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to V_{pr} during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings $+dV/-dV$ in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and V_d ($V_{pr} = K \cdot V_{dd}$, where $K = 1/3$ for the ideal MOS model) also provides: equal charge and discharge driver currents $I_{ch} = I_{dch}$, provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings dV in both charged and discharged bus during the data transfer phase P_{dtf} : $+dV = I_{ch} \cdot D_{dtf} / C_{LOAD}$; and $-dV = I_{dch} \cdot T_{dtf} / C_{LOAD}$. I_{ch} represents the driver pull up output current (which provides the C_{LOAD} charging from V_{pr} up to V_{dd}); I_{dch} represents the driver pull down output current (providing the C_{LOAD} discharging from V_{pr} up to V_{ss}); C_{LOAD} represents the bus lines' capacitances; $+dV$ represents the bus voltage change up from V_{pr} during data transfer phase; $-dV$ represents the bus voltage change down from V_{pr} during data transfer phase; and T_{dtf} represents the data transfer phase duration. The buses precharging to the specific level between ground and V_{dd} also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage V_{dd} (or

V_{cc}) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by $K \cdot V_{dd}$ and $(1-K) \cdot V_{dd}$ instead of simply V_{dd} . Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage V_{pr} and the deviation of the threshold voltage of the input transistors.

5 In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

10 Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.